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What is claimed is:

1. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first protection film formed to cover part of said first gate electrode,

wherein part of said first gate electrode which is not covered by said first protection film has a structure in which a first semiconductor layer and a first metal-semiconductor compound layer are stacked in this order on a first gate insulating film, and

the part of said first gate electrode which is covered by said first protection film has a structure in which said first semiconductor layer is formed on said first gate insulating film and said first metal-semiconductor compound layer is not formed on said first semiconductor layer.

2. The semiconductor storage device according to claim 1, further comprising a second protection film formed to cover part of said second gate electrode,

wherein part of said second gate electrode which is not covered by said second protection film has a structure in which a second semiconductor layer and a second metal-semiconductor compound layer are stacked in this order on a second gate

insulating film, and

the part of said second gate electrode which is covered by said second protection film has a structure in which said second semiconductor layer is formed on said second gate insulating film and said second metal-semiconductor compound layer is not formed on said second semiconductor layer.

3. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor.

4. The semiconductor storage device according to claim 3, further comprising a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said power supply.

5. The semiconductor storage device according to claim 3, further comprising a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said power supply.

6. The semiconductor storage device according to claim 3, further comprising:

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and a PMOS transistor having its gate electrode connected to said second power supply.

7. The semiconductor storage device according to claim 3, wherein said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

8. The semiconductor storage device according to claim 7, which comprises a

plurality of said first resistance-adding transistors.

9. The semiconductor storage device according to claim 3, wherein said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

10. The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

11. The semiconductor storage device according to claim 3, further comprising a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said word line.

12. The semiconductor storage device according to claim 3, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

13. The semiconductor storage device according to claim 3, further comprising:

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gate electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetween,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.